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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/387,109	08/31/1999	Matthew J. Adiletta	10559/079001	2177

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EXAMINER	
DILLER, JESSE DAVID	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/387,109	ADILETTA ET AL.	
	Examiner	Art Unit	
	Jesse Diller	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-12 and 14-18* is/are rejected.

7)☒ Claim(s) *5-8 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Examiner acknowledges receipt of the amendment in response to the office action dated 09/13/2004, which amendment was received 01/18/2005. At this point, claims 1-2, 5, 9, 11-12, 14-16, and 18 have been amended. Thus, claims 1-18 are still pending in the application.

Objections to the disclosure

2. In response to amendment, the objections to Figs. 1-5 of the Drawings are withdrawn. The objection to Fig. 5A is reiterated. See the objection in the section entitled "*Drawings.*"

3. In response to amendment, the objections to claims 2, 5, 9, 15, and 18 are withdrawn.

4. In the office action dated 09/13/2004, the disclosure was objected to because of the following informalities:

- On page 5, line 1, after "functional microengines", "(microengines)" should be deleted.
- On page 12, lines 18-20, after "performing," "a single cycle shift" should be replaced by "a".
- Page 24, lines 23-26 is unclear. A suggested changes is "Having issued as many references as early as possible, the goal would be to perform as many computations as possible in the microengines, in parallel with the references.

- Throughout the specification, the items designated "AMBA" and "Fbox" in the drawings are referred to as "ASB" and "microengine," respectively.

5. Throughout the specification, numerous other inconsistencies were noted. Applicant was encouraged to review the specification and correct any noted errors or inconsistencies. However, it appears that only the examples cited by the examiner were addressed. As previously noted, multiple inconsistencies remain throughout the specification. Applicant is again encouraged to carefully examine the disclosure to correct such inconsistencies.

Claim Rejections – 35 USC § 112 and 102

6. In response to amendment, the 35 USC § 112 rejections of claims 12, 14, 16 are withdrawn.

Response to Arguments

7. **Applicant's arguments filed** 1/18/2005 **with respect to the 35 USC §** 103 **rejections of claim** 1 **have been fully considered, and are persuasive.** Accordingly, the 35 USC 103 rejections of claims 1-4, 9-11, 14-18 are withdrawn. However, see the following action for new grounds of rejection:

DETAILED ACTION

8. Claims 1-18 are pending in the application, and have been examined.

Drawings

9. The drawings are objected to because:

- Fig. 5A appears to contain multiple errors. The lines in Fig. 5A are obviously misaligned, including a word wrap. This makes understanding of Fig. 5A very difficult.

10. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

Specification

11. In the office action dated 09/13/2004, the disclosure was objected to because of the following informalities:

- On page 5, line 1, after "functional microengines", "(microengines)" should be deleted.
- On page 12, lines 18-20, after "performing," "a single cycle shift" should be replaced by "a".
- Page 24, lines 23-26 is unclear. A suggested changes is "Having issued as many references as early as possible, the goal would be to perform as many computations as possible in the microengines, in parallel with the references.
- Throughout the specification, the items designated "AMBA" and "Fbox" in the drawings are referred to as "ASB" and "microengine," respectively.

12. Throughout the specification, numerous other inconsistencies were noted. Applicant was encouraged to review the specification and correct any noted errors or inconsistencies. However, it appears that only the examples cited by the examiner were addressed. As previously noted, multiple inconsistencies remain throughout the specification. For instance, the tables on pages 15-21 are misaligned, which could lead to printing and/or understanding errors if the application issues in its present form. Applicant is again encouraged to carefully examine the *entire* disclosure to correct such inconsistencies and errors.

13. In the amendment dated 1/18/2005, new drawings were submitted, and were numbered differently. However, the description of the drawings in the specification was not amended to reflect the changes and additions.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

NOTE: In the prior office action, it was recited, "For the purpose of prior art examination, 'microengine' has been taken to be synonymous with 'microcontrol functional unit.' Because applicant has not addressed this assertion, it is assumed that this definition is accepted.

15. **Claims 1, 3, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callemyn, U. S. Patent #5,115,507, in view of Chin, US Patent #6,286,083 and Nakagawa, U.S. Patent #5,701,434.**

16. **As for Claim 1, Callemyn discloses:**

- A controller for a random access memory (Fig. 3) comprising:
- A module (Registers REG A - REG D) that holds memory references (DPREQ, GPREQ, Fig. 1A) from a plurality of microcontrol functional units (DP, GP; also

see MA, MB, MC, Fig. 2, and P, MCLP, DCLP, in Fig. 3. These functional units have been taken as reading on "microcontrol functional unit.")

- A second r/w register holding memory references from a core processor, (Fig. 1A shows REG I holding memory request CPUREQ from a core processor CPU.) and
- Control logic (Fig. 1B shows a logic system) including an arbiter (Fig. 2) that looks at a status of the requests (Col. 2, lines 42-45 denotes priority as a status that determines the selection) and selects a memory reference from one of the registers (Col. 3, lines 30 and 36-38).

17. Callemyn does not disclose expressly

- A first read/write queue holding memory references from a computer bus;
- the modules or registers holding memory references are set up as queues, that
- the queue holding requests from the microcontrol units is an address and command queue, or that
- the arbiter makes a request selection on the basis of the fullness of the queues, as does the present invention.

18. Chin discloses a memory controller which arbitrates between memory references from multiple places, including a CPU (102, Fig. 1), bus (112, Fig. 1), and graphics controller (116, Fig. 1 via AGP bus 114). Chin teaches that his memory controller includes queues to hold the requests (250-272, Fig. 2), and control logic 242, Fig. 2, including an arbiter (300, Fig. 3D) that selects a memory reference from one of the queues.

19. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Callemyn allowing the memory controller to receive memory references from an external PCI computer bus, and to store the references in read and write queues, as does Chin, and to allow the memory references from the plurality of microcontrol functional units of Callemyn (graphics-related DP, GP, Fig. 1) to be sent through the APG bus of Chin

20. The motivation for doing so is taught by Chin on Col. 1, lines 25-30, namely that devices such as network interface cards, SCSI adapters, and audio cards often use such buses; it would be advantageous to have a computer system that allows the use of such devices.

21. Nakagawa discloses a random access memory controller (30, Fig. 1) which includes an address and command queue (Fig. 2 shows addresses and data (command) 711, in a single queue, Col. 5, line 42, holding all requests, both reads and writes, from multiple sources 10 and 20, Fig. 1 (see also Col. 2, line 54-55). He also discloses a queue control circuit 65, Fig. 3, which performs the function of an arbiter. Nakagawa teaches that his queue control circuit makes a selection from the queue based on an indication of the fullness or emptiness of the queue (Col. 5, lines 36-42 teach the fullness test.

22. Callemyn, Chin, and Nakagawa are analogous art because they are from the same field of endeavor, namely memory request controllers.

23. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Callemyn and Chin by storing requests in queues. The

motivation for doing so is taught by Nakagawa. He notes the conventional use of a FIFO queue for access sequence assurance (Col. 1, lines 48-50). Access sequence assurance ensures that dependant instructions are not scrambled.

24. At the time of the invention it would also have been obvious to a person of ordinary skill in the art to modify Callemyn and Chin by combining registers A-D into a single queue holding references from multiple sources, and to combine the separate read and write queues into one read/write queue, as does Nakagawa. In Col. 2, lines 1-8, Nakagawa teaches as motivation that a single common queue (instead of multiple queues) reduces the scale of the queue structure, and also eliminates the need to provide dedicated entries in an integral multiple of the number of queues. In Col. 5, lines 62-66 also note that the number of queue entries is reduced, which allows the entire circuit to be made smaller, accommodated on a single LSI. As a result, the wiring length is shortened, which in turn shortens the turnaround delay.

25. Lastly, at the time of the invention it would have been obvious to a person of ordinary skill in the art to add the selection technique disclosed by Nakagawa to the memory controller disclosed by Callemyn and Chin. The motivation for checking the fullness of the queue is obvious. If the queue is full, no entries can be added to it, and a selection must be made from that queue before any more commands can be processed by the system. If the queue is empty, no selection can be made and information must be added before another selection can be made. Nakagawa recognizes this, and his arbiter, if the queue is full, sends a signal to the request sources suppressing any

further requests. (Col 4, lines 5-9) If the queue entry is empty, he sends a priority signal that ensures that a memory request will be written into the queue.

26. Therefore, it would have been obvious to add the computer bus and associated queues of Chin with the controller of Callemyn, and to combine the use of queues, the single queue structure and the fullness checking scheme of Nakagawa with the controller of Callemyn and Chin, for the benefit of access sequence assurance and reduced complexity, size, and turnaround time, as well as support for external expansion devices, to obtain the invention as specified in claim 1.

27. **As for claim 3, Callemyn discloses** that his arbitration system includes a register dedicated to high priority tasks (SL.EX, Fig. 2; REG B and D, Fig. 1A show block requests directed to exclusive queues; see also Col. 1, lines 50-55).

28. **As for claims 9 and 10, Callemyn discloses** a DRAM Controller CT.DRAM in Fig. 3. The limitations of claims 9 and 10 are inherent in a DRAM controller. A random access memory requires certain control signals to function correctly. Therefore, any memory control system must include means for generating memory control signals that will adequately meet the demands of the memory module. As an example, see Callemyn, US Patent #4,991,112, hereinafter CALLEMYN, not to be confused with the primary reference, Callemyn, US Patent #5,115,507. In Fig. 1, CALLEMYN discloses the same structure as the primary reference. In Fig. 2, CALLEMYN discloses that his DRAM controller includes an address control module AD.CTRL. In Col. 6, lines 26-38, he teaches that this module is responsive to an address corresponding to the selected request REQS, Fig. 2, and that the module produces an address (lines 35-36), as well

as commands to control a memory interface (lines 41-42 disclose memory selection signals; Fig. 2 shows these signals controlling a memory control module MEM CTRL). The memory control module MEM CTRL is responsive to received signals and produces memory control signals.

29. **Claims 2 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callemyn, Chin, and Nakagawa, further in view of Hansen, U. S. Patent #4,788,640.**

30. **As for claim 2, Callemyn, Chin, and Nakagawa teach** all the limitations of claim 1, as described above. Callemyn additionally teaches that the selection of requests is based on a priority (Col. 2, lines 43-44). He also teaches that the priorities may be programmed (Col. 1, lines 59-60; Col 2, lines 41-43). Fig. 1A shows VAL-REG, which determines the priorities (Col 2, lines 41-43). Callemyn, Chin, and Nakagawa do not, however, expressly disclose that the programmable request selection command is stored in a priority service control register, as does claim 2.

31. Hansen, US Patent #4,788,640, included in Callemyn by reference (Callemyn, Col. 2, line 25), discloses a memory interface (Fig. 1), which includes a priority logic unit (10, Fig. 1; Col. 3, line 47). The priority logic unit contains registers (41-43, Fig. 2) that store a programmable priority value, which values determine the order of incoming memory requests (Col. 1, lines 47-50).

32. Callemyn, Chin, Nakagawa, and Hansen are analogous art, because they belong to the same field of endeavor, namely memory controllers which endeavor to decrease the memory access bottleneck in computer systems.

33. At the time of the invention it would have been obvious to a person of ordinary skill in the art to add the programmable priority control register taught by Hansen to the system of Callemyn, Chin, and Nakagawa described above. The motivation for doing so is described by Hansen in Col. 1, lines 50-55, namely, that it increases the flexibility of the system, allowing the system designer to choose the tradeoff between bus latency versus bus speed and performance.

34. Therefore, it would have been obvious to add the priority service control register taught by Hansen to Callemyn, Chin, and Nakagawa, for the benefit of allowing programmable adjustment of request handling and system design flexibility, to obtain the invention as specified in claim 2.

35. **As for claim 14,** Callemyn, Chin, and Nakagawa do not teach the limitation that the arbitration policy favors chained microengine memory references. Hansen teaches, however, that his system operates in a first priority level when processing non-chained memory requests, and shifts to a second level when a chained or block request is detected (Col. 1, lines 45-50). Hansen teaches that by programming the priority levels, uninterruptible block transfers may be accomplished (lines 51-53; see also Col. 5, lines 37-44), meaning that the chained requests are given a higher priority, or are, in the language of claim 14, favored.

36. At the time of the invention it would have been obvious to a person of ordinary skill in the art to add the arbitration policy favoring chained requests as taught by Hansen to the system of Callemyn, Chin, and Nakagawa described above. The motivation for doing so is described by Hansen in Col. 1, lines 22-27 and 50-55, namely,

that block transfers increase the speed of the acquisition rate and improve the bus speed and performance. Therefore, it would have been obvious to add the arbitration policy favoring chained requests as taught by Hansen to Callemyn, Chin, and Nakagawa, for the benefit of increasing bus speed and performance, to obtain the invention as specified in claim 14.

37. **As for claim 15**, Callemyn, Chin, and Nakagawa do not teach the limitation that the arbitration policy services chained microengine memory references until a chain bit is cleared. Hansen teaches, however, that by programming the priority levels, uninterruptible block transfers may be accomplished (Col. 1, lines 51-53; see also Col. 5, lines 37-44), meaning that the chained requests are given a higher priority, and are serviced until completion, at which time a chain detection signal (45, Fig. 2) is cleared.

38. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow chained requests to be serviced until completion. The motivation for doing so is obvious, namely that interrupting a block transfer defeats the purpose of the block transfer. The improvements in speed gained by not interrupting the block transfer is the reason for having a block transfer in te first place. Therefore, it would have been obvious to add the arbitration policy completely servicing chained requests as taught by Hansen to Callemyn, Chin, and Nakagawa, for the benefit of increasing bus speed and performance, to obtain the invention as specified in claim 14.

39. **As for claim 16**, Callemyn, Chin, and Nakagawa do not teach the limitation that the arbitration policy starts by looking for chained microengine memory references.

Hansen teaches, however, that his system is activated as soon as block requests are detected (Col. 2, lines 1-3).

40. At the time of the invention it would have been obvious to a person of ordinary skill in the art to add the arbitration policy favoring chained requests as taught by Hansen to the system of Callemyn, Chin, and Nakagawa described above. The motivation for doing so is described by Hansen in Col. 1, lines 22-27 and 50-55, namely, that block transfers increase the speed of the acquisition rate and improve the bus speed and performance. Therefore, it would have been obvious to add the arbitration policy favoring chained requests as taught by Hansen to Callemyn, Chin, and Nakagawa, for the benefit of increasing bus speed and performance, to obtain the invention as specified in claim 16.

41. **As for claim 17,** Callemyn, Chin, and Nakagawa do not teach the limitation that the arbitration policy services chained microengine memory references completely. Hansen teaches, however, that by programming the priority levels, uninterruptible block transfers may be accomplished (Col. 1, lines 51-53; see also Col. 5, lines 37-44), meaning that the chained requests are given a higher priority, and are serviced until completion.

42. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow chained requests to be serviced until completion. The motivation for doing so is obvious, namely that interrupting a block transfer defeats the purpose of the block transfer. Therefore, it would have been obvious to add the arbitration policy completely servicing chained requests as taught by Hansen to Callemyn, Chin, and

Nakagawa, for the benefit of increasing bus speed and performance, to obtain the invention as specified in claim 17.

43. **As for claim 18,** Callemyn, Chin, and Nakagawa do not teach the limitation that when a chain bit is set, the arbitration engine services the same queue again until the chain bit is cleared. Hansen teaches, however, that by programming the priority levels, uninterruptible block transfers may be accomplished (Col. 1, lines 51-53; see also Col. 5, lines 37-44), meaning that the chained requests are given a higher priority, and are serviced until completion. While the chained request indicator (45, Fig. 2) is set, the arbitration engine services the same request source again (Fig. 4b).

44. At the time of the invention it would have been obvious to a person of ordinary skill in the art to service the same request source repetitively, while performing a block transfer. The motivation for doing so is obvious, namely that a block transfer is made up of consecutive requests from the same source. Therefore, it would have been obvious to add the process of repetitively servicing the requesting source during service of chained requests as taught by Hansen to Callemyn, Chin, and Nakagawa, for the benefit of performing block transfers, to obtain the invention as specified in claim 18.

45. **Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Callemyn, Chin, and Nakagawa, further in view of Bratt, U. S. Patent #5,740,402.**

46. Callemyn, Chin, and Nakagawa teach all the limitations of claim 1, as described above. Callemyn, Chin, and Nakagawa do not expressly teach, however, that the address and command queue comprises an even and odd bank queue, or that a microengine sorts the memory references into odd and even references.

47. Bratt, US Patent #5,740,402, discloses a memory reference pipeline that handles simultaneous memory references (Col. 2, lines 29-31, 36-37). His apparatus includes:

- a microengine 202, Fig. 2, that sorts memory references into even/odd bank references (Fig. 3 shows microengine 202, Fig. 2; including multiple request sources 300 and 302, and logic 310 to sort references into even/odd references. Fig. 2 shows the output of the microengine going to even/odd pipelines).
- Even and odd bank queues (210, Fig. 2).

48. Callemyn, Chin, Nakagawa, and Bratt are analogous art because they are from the same field of endeavor, namely devices that manage memory references to improve the performance of computer systems.

49. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include the even and odd bank queues and reference sorting engine disclosed by Bratt in the combination of Callemyn, Chin, and Nakagawa as described above. The motivation for doing so is taught by Bratt. In Col. 1, lines 28-40 teach that interleaving memory systems can increase the effective speed of accessing large memory systems (28-31). Col. 1, lines 48-64 teach that interleaving memory allows execution of more than one instruction per cycle, increasing the effective memory bandwidth.

50. Therefore, it would have been obvious to modify the combination of Callemyn, Chin, and Nakagawa as disclosed above to include the even and odd bank queues and sorting microengine disclosed by Bratt, for the benefit of increasing effective memory bandwidth, to obtain the invention as specified in claim 4.

51. **Claim 11 is rejected as being unpatentable over Callemyn, Chin, and Nakagawa, further in view of Byers, U. S. Patent #5,784,712.**

52. Callemyn, Chin, and Nakagawa disclose all the limitations of claim 1, as set forth above. They do not disclose expressly that the control logic is responsive to a chaining bit that when set allows special handling of contiguous memory references.

53. Byers, US Patent #5,784,712, discloses that a memory request may have bits that denote a block or chained memory request (966, Fig. 12 – bits set to '11' denotes autoincrement; Col. 3, lines 46-49 notes that autoincrement is used for block, i.e., contiguous, or chained, requests). Col. 3, lines 38-42 teaches that for chained requests, the processor need not provide an address for each read/write operation.

54. Byers, Callemyn, Chin, and Nakagawa are analogous art, because they are from the same field of endeavor, namely memory request handling systems.

55. At the time of the invention it would have been obvious to one skilled in the art to add the chained request bits and special handling disclosed by Byers to the combination of Callemyn, Chin, and Nakagawa. The motivation for doing so is taught by Byers, in Col. 3, lines 47-66. The special handling may free up the processor or requesting functional unit to do other tasks while the contiguous requests are being handled. Also, since it does not have to issue as many addresses to the memory system, the processor may be free to perform other tasks while the chained transfer is being completed.

56. Therefore, it would have been obvious to combine Byers with the combination of Callemyn, Chin, and Nakagawa, for the benefit of allowing the requesting entity to perform more work, to obtain the invention as specified in claim 11.

Allowable Subject Matter

57. Claims 5-8 and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and resolving any other outstanding issues.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse Diller whose telephone number is (571)272-4173. After October 19, the examiner will be able to be reached at the Carlyle, Alexandria campus at (571) 272-4173. The examiner can normally be reached on 8:30AM-5:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can presently be reached on (571)272-4201 or, after October 19, at (571) 272-4201. The fax phone number for the organization where this application or proceeding is currently assigned is 703-872-9306. The central telephone number for the Technology Center is (571)272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JD

DONALD SPARKS
SUPERVISORY PATENT EXAMINER